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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,487	02/10/2004	Ho-Yuan Yu	065860-5002US	3256

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
01/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,487	YU, HO-YUAN	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-20* is/are allowed.

6)☒ Claim(s) *21-24 and 26-34* is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 30th, 2007 has been entered. A new rejection is made as set forth in this Office Action. Claims (15-34) are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 21-24 and 26-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Darwish (U.S. Patent 6,764,906).

In re claim 21, **Darwish** discloses a method for fabricating a dual gate structure for a field effect transistor (FET), the method comprising: in sequence, etching a gate trench in a surface of a semiconductor substrate **100, 102**; forming a first gate region **124A** at the bottom of the gate trench; implanting a buffer region 124B beneath the first gate region **124A**; and implanting (see col. 9, lines 2-19 and FIGS. 17A-B and 18) a

second gate region **124C** beneath the buffer region **124B**, wherein the second gate region **124C** is formed entirely beneath the first gate region **124A**; wherein said first gate region **124A** and said second gate region **124C** together form said dual gate structure (see col. 7, line 55 to col. 8, line 10 and FIG. 18, for example).

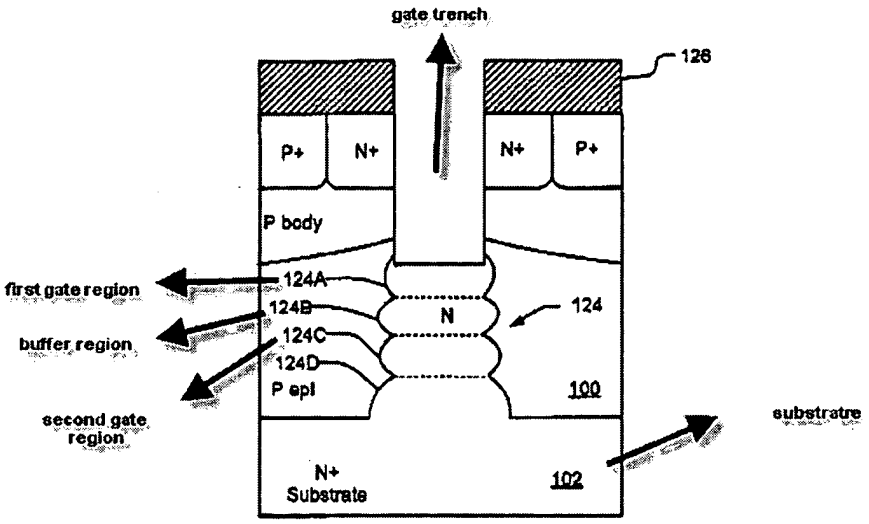

Fig. 18

In re claim 22, as applied to claim 21 above, **Darwish** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the first gate region **124A** (see FIG. 5G and 18, for example).

In re claim 23, as applied to claim 21 above, **Darwish** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the buffer region **124B** (see FIG. 5G and 18, for example).

In re claim 24, as applied to claim 21 above, **Darwish** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the second gate region **124C** (see FIG. 5G and 18, for example).

In re claim 26, **Darwish** discloses a method for fabricating a dual gate structure for a field effect transistor (FET), the method comprising: etching a gate trench in a surface of a semiconductor substrate **100, 102**; forming a first gate region **124A** at the bottom of the gate trench, implanting a buffer region **124B** beneath the first gate region **124A**; and implanting (see col. 9, lines 2-19 and FIGS. 17A-B and 18) a second gate region **124C** beneath the buffer region **124B**, wherein the second gate region **124C** is formed entirely beneath the first gate region **124A**; wherein said first gate region **124A** and said second gate region **124C** together form said dual gate structure (see col. 7, line 55 to col. 8, line 10 and FIG. 18, for example).

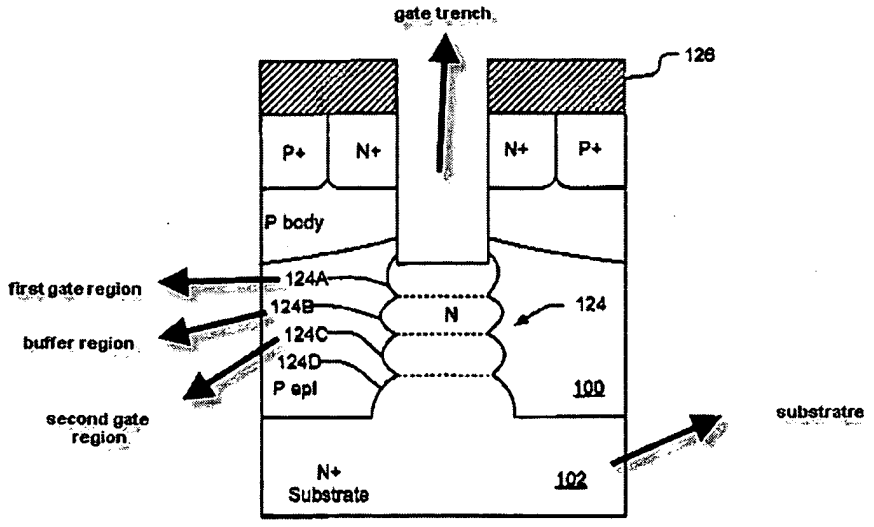

Fig. 18

In re claim 27, as applied to claim 26 above, **Darwish** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the first gate region **124A** (see FIGS. 5G and 18, for example).

In re claim 28, as applied to claim 26 above, **Darwish** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the buffer region **124B** (see FIGS. 5G and 18, for example).

In re claim 29, as applied to claim 26 above, **Darwish** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the second gate region **124C** (see FIGS. 5G and 18, for example).

In re claim 30, **Darwish** discloses a method for fabricating a dual gate structure for a field effect transistor the method comprising: etching a gate trench in a surface of a semiconductor substrate **100, 102** (see FIG. 18);

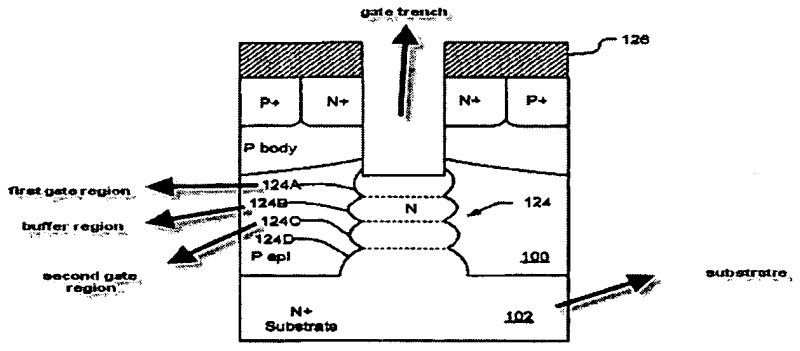

Fig. 18

forming a first gate region **124A** at the bottom of the gate trench; implanting a buffer region **124B** beneath the first gate region **124A**; and after implanting the buffer region **124B**, implanting (see col. 9, lines 2-19 and FIGS. 17A-B and 18) a second gate region **124C** beneath the buffer region **124B**, wherein said second gate region **124C** is formed entirely beneath said first gate region **124A**; wherein said first gate region **124A** and said second gate region **124C** together form said dual gate structure (see col. 7, line 55 to col. 8, line 10 and FIG. 18, for example).

In re claim 31, as applied to claim 30 above, **Darwish** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the first gate region **124A** (see FIGS. 5G and 18, for example).

In re claim 32, as applied to claim 30 above, **Darwish** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the buffer region **124B** (see FIGS. 5G and 18, for example).

In re claim 33, as applied to claim 30 above, **Darwish** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the second gate region **124C** (see FIGS. 5G and 18, for example).

In re claim 34, as applied to claim 30 above, **Darwish** discloses all claimed limitations including the limitation wherein the method further comprising forming a first sidewall spacer to establish a width of the buffer region **124B**, and forming a second

sidewall spacer to establish a width of the second gate region **124C**, wherein the second sidewall spacer is thicker than the first sidewall spacer (see FIGS. 5G and 18, for example).

Allowable Subject Matter

4. Claims 15-20 were previously allowed over prior art of record as indicated in Office Action No. 20061109 mailed on November 13th, 2006.

5. Claim 25 was previously objected to as indicated in Office Action No. 20061109 mailed on November 13th, 2006 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Applicants' Amendment and Arguments

6. Applicant's arguments with respect to claims 15-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Khiem D. Nguyen/
Examiner, Art Unit 2823

/KN/